REMARKS

The Examiner is thanked for the indication that claims 13-19 and 28-29 would be allowable if rewritten to overcome rejections under 35 U.S.C. §112, first paragraph, and to include all of the limitations of the base claim and any intervening claims.

Claims 1-29 are pending in the application. Claims 1, 5, 9, 20, and 24 are independent. No claims have been amended, canceled, or added. The Specification has been amended. These changes are believed to introduce no new matter and their entry is respectfully requested.

Rejection of Claims 1, 3-5, and 7-8 Under Obviousness-Type Double Patenting

In the Office Action, the Examiner rejected claims 1, 3-5, and 7-8 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,662,278 to Khan et al. (hereinafter "Khan"). Applicants respectfully traverse the rejection.

In papers filed herewith, Applicants have submitted a Terminal Disclaimer disclaiming the terminal part of any patent granted on the above-identified application that would extend beyond the expiration of the full statutory term of United States Patent No. 6,662,278. Applicants respectfully submit that the Terminal Disclaimer overcomes the obviousness-type double patenting rejection. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection to claims 1, 3-5, and 7-8.

Rejection of Claims 9-12, 20-24, and 26-27 Under Obviousness-Type Double Patenting

In the Office Action, the Examiner rejected claims 9-12, 20-24, and 26-27 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,662,278 to Khan et al. (hereinafter "Khan"). Applicants respectfully traverse the rejection.

In papers filed herewith, Applicants have submitted a Terminal Disclaimer

disclaiming the terminal part of any patent granted on the above-identified application that would extend beyond the expiration of the full statutory term of United States Patent No. 6,662,278. Applicants respectfully submit that the Terminal Disclaimer overcomes the obviousness-type double patenting rejection. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection to claims 9-12, 20-24, and 26-27.

Rejection of Claims 9, 13-19, 24, and 28-29 Under 35 U.S.C. §112, First Paragraph

In the Office Action, the Examiner rejected claims 9, 13-19, 24, and 28-29 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Specifically, the Examiner asserts that no support was found in the Specification for a processor having an original percentage of memory bandwidth allocated to it (claims 9 and 24) and that no support was found in the Specification for a graphics memory or I/O device having an original percentage of memory bandwidth allocated to it, etc. Applicants respectfully traverse the rejection.

Claim 9 recites in pertinent part "a processor having an original percentage of memory bandwidth or number of memory accesses allocated to it." Claim 24 recites in pertinent part "allocating to a processor an original percentage of memory bandwidth or number of memory accesses." Paragraph **[0021]** of Applicants' Specification describes "Figure 1 depicts a method 100 to throttle memory according to an embodiment of the present invention." Paragraph **[0027]** describes "Figure 2 is a block diagram of a computer system 200 suitable for implementing the method 100. The computer system 200 includes a ***processor 202***...." Paragraph **[0022]** describes "Step 104 applies a mask to ***allocate memory bandwidth***. .... In other words, the mask defines the ***number*** and pattern of ***memory accesses***" (emphasis added). Thus, Applicants respectfully submit that the Specification sufficiently describes "a processor having an original percentage of memory bandwidth or number of memory accesses allocated to it" as recited in claim 9 and "allocating to a processor an original percentage of memory bandwidth or number of memory accesses" as recited in claim 24.

Claim 13 recites in pertinent part "***a graphics memory having an original percentage*** of graphics memory bandwidth or number of graphics memory accesses allocated to it; and a ***graphics controller to increase the percentage*** of graphics memory bandwidth or the number of graphics memory accesses allocated to the graphics memory when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the graphics memory, ***the graphics controller further to decrease the percentage*** of graphics memory bandwidth or the number of graphics memory accesses allocated to the graphics memory when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the graphics memory" (emphasis added).

Paragraph **[0021]** of Applicants' Specification describes "Figure 1 depicts a method 100 to throttle memory according to an embodiment of the present invention." Paragraph **[0027]** describes "Figure 2 is a block diagram of a computer system 200 suitable for implementing the method 100. Paragraph **[0029]** describes the computer system 200 as having "a graphics controller 206" and paragraph **[0041]** describes the computer system 200 as having "a graphics local memory 230."

Paragraph **[0022]** describes "Step 104 applies a mask to ***allocate memory bandwidth***. In one embodiment, the mask sets the specific clock cycles in which memory accesses can proceed to memory. In other words, the mask defines the ***number*** and pattern of ***memory accesses***" (emphasis added).

Paragraph **[0050]** of Applicants' Specification describes "In another embodiment, the ***masking tool 290*** is located in the graphics local memory 230 (or ***the graphics controller*** 206) and ***controls the bandwidth of the graphics local memory*** 230" (emphasis added). Thus, Applicants respectfully submit that the Specification sufficiently describes the subject matter recited in claim 13 and respectfully request that the Examiner reconsider and remove the rejection.

Claim 14 recites in pertinent part "***an individual I/O device having an original percentage of graphics memory bandwidth*** or number of graphics memory accesses allocated to it, the graphics controller to increase the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to the one or more I/O devices when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the one or more I/O devices, ***the graphics controller further to decrease the percentage*** of graphics memory bandwidth or the number of graphics memory accesses allocated to the one or more I/O devices when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the one or more I/O devices" (emphasis added).

Paragraph **[0021]** of Applicants' Specification describes "Figure 1 depicts a method 100 to throttle memory according to an embodiment of the present invention." Paragraph **[0027]** describes "Figure 2 is a block diagram of a computer system 200 suitable for implementing the method 100. Paragraph **[0029]** describes the computer system 200 as having a "graphics controller 206," paragraph **[0038]** describes the computer system 200 as having "I/O devices 226" and paragraph **[0041]** describes the computer system 200 as having "a graphics local memory 230."

Paragraph **[0022]** describes "Step 104 applies a mask to ***allocate memory bandwidth***. In one embodiment, the mask sets the specific clock cycles in which memory accesses can proceed to memory. In other words, the mask defines the ***number*** and pattern of ***memory accesses***" (emphasis added). Paragraph **[0048]** of Applicants' Specification describes "In one embodiment, the main memory 224 includes ***a masking tool 290 to allow read and write requests*** to reach memory ***from*** the processor 202, the ***I/O devices*** 226, the graphics controller 206, etc." Paragraph **[0050]** of Applicants' Specification describes "In another embodiment, the ***masking tool 290*** is located in the graphics local memory 230 (or ***the***

graphics controller 206) and ***controls the bandwidth*** of the graphics local memory 230" (emphasis added).

Paragraph [**0016**] of Applicants' Specification describes "***Reference*** throughout this specification ***to "one embodiment" or "an embodiment"*** means that a particular feature, structure, or characteristic described in connection with the embodiment ***is included in at least one embodiment*** of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are ***not necessarily*** all referring ***to the same embodiment***" (emphasis added). Thus, Applicants respectfully submit that the Specification sufficiently describes the subject matter recited in claim 14 and respectfully request that the Examiner reconsider and remove the rejection.

Claim 15 recites in pertinent part "***the processor*** further ***includes an original percentage of graphics memory bandwidth*** or number of graphics memory accesses allocated to it, ***the graphics controller to increase the percentage*** of graphics memory bandwidth or the number of graphics memory accesses allocated to the processor when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the processor, ***the graphics controller further to decrease the percentage*** of graphics memory bandwidth or the number of graphics memory accesses allocated to the processor when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the processor" (emphasis added).

Paragraph [**0021**] of Applicants' Specification describes "Figure 1 depicts a method 100 to throttle memory according to an embodiment of the present invention." Paragraph [**0027**] describes "Figure 2 is a block diagram of a computer system 200 suitable for implementing the method 100. Paragraph [**0029**] describes the computer system 200 as having a "graphics controller 206," paragraph [**0027**] describes the computer system 200 as

having "a processor 202" and paragraph **[0041]** describes the computer system 200 as having "a graphics local memory 230."

Paragraph **[0022]** describes "Step 104 applies a mask to ***allocate memory bandwidth***. In one embodiment, the mask sets the specific clock cycles in which memory accesses can proceed to memory. In other words, the mask defines the ***number*** and pattern of ***memory accesses***" (emphasis added). Paragraph **[0048]** of Applicants' Specification describes "In one embodiment, the main memory 224 includes ***a masking tool 290 to allow read and write requests*** to reach memory ***from the processor*** 202, the I/O devices 226, the graphics controller 206, etc." Paragraph **[0050]** of Applicants' Specification describes "In another embodiment, the ***masking tool 290*** is located in the graphics local memory 230 (or ***the graphics controller*** 206) and ***controls the bandwidth*** of the graphics local memory 230" (emphasis added).

Paragraph **[0016]** of Applicants' Specification describes "***Reference*** throughout this specification ***to "one embodiment" or "an embodiment"*** means that a particular feature, structure, or characteristic described in connection with the embodiment ***is included in at least one embodiment*** of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are ***not necessarily*** all referring ***to the same embodiment***" (emphasis added). Thus, Applicants respectfully submit that the Specification sufficiently describes the subject matter recited in claim 15 and respectfully request that the Examiner reconsider and remove the rejection.

Claim 16 recites in pertinent part "wherein the chipset further comprises ***a graphics memory having an original percentage of*** graphics memory bandwidth or number of graphics memory accesses allocated to it, the ***graphics memory to increase the percentage of*** graphics memory bandwidth or the number of graphics memory accesses allocated to itself when an actual percentage of graphics memory bandwidth or number of graphics memory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to itself, ***the graphics memory further to decrease the percentage of*** graphics memory bandwidth or the number of graphics memory accesses

allocated to itself when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to itself" (emphasis added).

Paragraph **[0021]** of Applicants' Specification describes "Figure 1 depicts a method 100 to throttle memory according to an embodiment of the present invention." Paragraph **[0027]** describes "Figure 2 is a block diagram of a computer system 200 suitable for implementing the method 100. Paragraph **[0029]** describes the computer system 200 as having "a graphics controller 206" and paragraph **[0041]** describes the computer system 200 as having "a graphics local memory 230."

Paragraph **[0022]** describes "Step 104 applies a mask to ***allocate memory bandwidth***. In one embodiment, the mask sets the specific clock cycles in which memory accesses can proceed to memory. In other words, the mask defines the ***number*** and pattern of ***memory accesses***" (emphasis added). Paragraph **[0050]** of Applicants' Specification describes "In another embodiment, the ***masking tool 290*** is located in ***the graphics local memory*** 230 (or the graphics controller 206) and ***controls the bandwidth of the graphics local memory*** 230" (emphasis added). Thus, Applicants respectfully submit that the Specification sufficiently describes the subject matter recited in claim 16 and respectfully request that the Examiner reconsider and remove the rejection.

Claim 17 recites in pertinent part "***an individual I/O device having an original percentage of graphics memory bandwidth*** or number of graphics memory accesses allocated to it, ***the graphics memory to increase the percentage*** of graphics memory bandwidth or the number of graphics memory accesses allocated to the one or more I/O devices when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the one or more I/O devices, ***the graphics memory further to decrease the percentage*** of graphics memory bandwidth or the number of graphics memory accesses allocated to the one or more I/O devices when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more

than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the one or more I/O devices" (emphasis added).

Paragraph **[0021]** of Applicants' Specification describes "Figure 1 depicts a method 100 to throttle memory according to an embodiment of the present invention." Paragraph **[0027]** describes "Figure 2 is a block diagram of a computer system 200 suitable for implementing the method 100. Paragraph **[0038]** describes the computer system 200 as having "I/O devices 226" and paragraph **[0041]** describes the computer system 200 as having "a graphics local memory 230."

Paragraph **[0022]** describes "Step 104 applies a mask to ***allocate memory bandwidth***. In one embodiment, the mask sets the specific clock cycles in which memory accesses can proceed to memory. In other words, the mask defines the ***number*** and pattern of ***memory accesses***" (emphasis added). Paragraph **[0048]** of Applicants' Specification describes "In one embodiment, the main memory 224 includes ***a masking tool 290 to allow read and write requests*** to reach memory ***from*** the processor 202, the ***I/O devices*** 226, the graphics controller 206, etc."

Paragraph **[0050]** of Applicants' Specification describes "In another embodiment, the ***masking tool 290*** is located in the ***graphics local memory*** 230 (or the graphics controller 206) and ***controls the bandwidth*** of the graphics local memory 230" (emphasis added). Paragraph **[0016]** of Applicants' Specification describes "***Reference*** throughout this specification ***to "one embodiment" or "an embodiment"*** means that a particular feature, structure, or characteristic described in connection with the embodiment ***is included in at least one embodiment*** of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are ***not necessarily*** all referring ***to the same embodiment***" (emphasis added). Thus, Applicants respectfully submit that the Specification sufficiently describes the subject matter recited in claim 17 and respectfully request that the Examiner reconsider and remove the rejection.

Claim 18 recites in pertinent part "wherein ***the processor further includes an original percentage of graphics memory bandwidth*** or number of graphics memory accesses allocated to it, ***the graphics memory to increase the percentage*** of graphics memory bandwidth or the number of graphics memory accesses allocated to the processor when an actual percentage of graphics memory bandwidth or number of graphics memory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the processor, ***the graphics memory further to decrease the percentage*** of graphics memory bandwidth or the number of graphics memory accesses allocated to the processor when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the processor" (emphasis added).

Paragraph **[0021]** of Applicants' Specification describes "Figure 1 depicts a method 100 to throttle memory according to an embodiment of the present invention." Paragraph **[0027]** describes "Figure 2 is a block diagram of a computer system 200 suitable for implementing the method 100. Paragraph **[0027]** describes the computer system 200 as having "a processor 202" and paragraph **[0041]** describes the computer system 200 as having "a graphics local memory 230."

Paragraph **[0022]** describes "Step 104 applies a mask to ***allocate memory bandwidth***. In one embodiment, the mask sets the specific clock cycles in which memory accesses can proceed to memory. In other words, the mask defines the ***number*** and pattern of ***memory accesses***" (emphasis added). Paragraph **[0048]** of Applicants' Specification describes "In one embodiment, the main memory 224 includes ***a masking tool 290 to allow read and write requests*** to reach memory ***from the processor*** 202, the I/O devices 226, the graphics controller 206, etc." Paragraph **[0050]** of Applicants' Specification describes "In another embodiment, the ***masking tool 290*** is located in the ***graphics local memory*** 230 (or the graphics controller 206) and ***controls the bandwidth*** of the graphics local memory 230" (emphasis added).

Paragraph [**0016**] of Applicants' Specification describes "***Reference*** throughout this specification ***to "one embodiment" or "an embodiment"*** means that a particular feature, structure, or characteristic described in connection with the embodiment ***is included in at least one embodiment*** of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are ***not necessarily*** all referring ***to the same embodiment***" (emphasis added). Thus, Applicants respectfully submit that the Specification sufficiently describes the subject matter recited in claim 18 and respectfully request that the Examiner reconsider and remove the rejection.

Claim 19 recites in pertinent part "wherein the chipset further comprises ***one or more input/output (I/O) devices having an original percentage of memory bandwidth*** or number of memory accesses allocated to it, wherein ***the memory controller is to increase the percentage*** of memory bandwidth or the number of memory accesses allocated to the one or more I/O devices when an actual percentage of memory bandwidth or number of memory accesses by the one or more I/O devices is less than the original percentage of memory bandwidth or number of memory accesses allocated to the one or more I/O devices, ***the memory controller further to decrease the percentage*** of memory bandwidth or the number of memory accesses allocated to the one or more I/O devices when the actual percentage of memory bandwidth or number of memory accesses by the one or more I/O devices is more than the original percentage of memory bandwidth or number of memory accesses allocated to the one or more I/O devices" (emphasis added).

Paragraph [**0021**] of Applicants' Specification describes "Figure 1 depicts a method 100 to throttle memory according to an embodiment of the present invention." Paragraph [**0027**] describes "Figure 2 is a block diagram of a computer system 200 suitable for implementing the method 100. Paragraph [**0030**] describes the computer system 200 as having "a memory controller 208," and paragraph [**0037**] describes the computer system 200 as having "main memory 224," paragraph [**0038**] describes the computer system 200 as having "I/O devices 226," and paragraph [**0041**] describes the computer system 200 as having "a graphics local memory 230."

Paragraph [**0022**] describes "Step 104 applies a mask to ***allocate memory bandwidth***. In one embodiment, the mask sets the specific clock cycles in which memory accesses can proceed to memory. In other words, the mask defines the ***number*** and pattern of ***memory accesses***" (emphasis added). Paragraph [**0048**] of Applicants' Specification describes "In one embodiment, the main memory 224 includes ***a masking tool 290 to allow read and write requests*** to reach memory ***from*** the processor 202, the ***I/O devices*** 226, the graphics controller 206, etc." Paragraph [**0049**] of Applicants' Specification describes "Alternatively, the ***masking tool*** 290 can be located ***in*** the ***memory controller*** 208" (emphasis added).

Paragraph [**0016**] of Applicants' Specification describes "***Reference*** throughout this specification ***to "one embodiment" or "an embodiment"*** means that a particular feature, structure, or characteristic described in connection with the embodiment ***is included in at least one embodiment*** of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are ***not necessarily*** all referring ***to the same embodiment***" (emphasis added). Thus, Applicants respectfully submit that the Specification sufficiently describes the subject matter recited in claim 19 and respectfully request that the Examiner reconsider and remove the rejection.

Rejection of Claims 1-12 and 20-27 Under 35 U.S.C. §103(a)

In paragraph 6 of the Office Action, the Examiner rejected claims 1-2, 4-6, and 8 and under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 5,953,685 to Bogin et al. (hereinafter "Bogin") in view of U.S. Patent No. 6,021,076 to Woo et al. (hereinafter "Woo"). To establish a *prima facie* case of obviousness, an Examiner must show that that there is some suggestion or motivation to modify a reference to arrive at the claimed invention, that there is some expectation of success, and that the cited reference teaches each and every element of the claimed invention. (MPEP §2143) *citing In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir.1991)). Applicants respectfully traverse the rejection.

Representative independent claim 1 recites in pertinent part "increasing the bandwidth or number of accesses allocated to the processor to a percentage higher than the original percentage of bandwidth or number of accesses allocated when accesses to memory

by the processor are less than the original percentage of bandwidth or number of accesses allocated to the processor; and decreasing the bandwidth or number of accesses allocated to the processor to a percentage lower than an original bandwidth or number of accesses allocated when accesses to memory by the processor are ***more than*** the original percentage of bandwidth or number of accesses allocated to the processor " (emphasis added). These elements are not disclosed in disclosed in the combination of Bogin and Woo.

Moreover, the Examiner does not assert that these elements are taught or reasonably suggested by the combination of Bogin and Woo. The Examiner asserts that Bogin fails to disclose increasing the allocated bandwidth or number of accesses when the actual bandwidth or number of accesses is ***less than*** the originally allocated bandwidth or number of access and that Woo teaches increasing the allocated bandwidth or number of accesses when the actual bandwidth or number of accesses is ***less than*** the originally allocated bandwidth or number of access. Applicants respectfully submit that even if Woo teaches increasing the allocated bandwidth or number of accesses when the actual bandwidth or number of accesses is less than the originally allocated bandwidth or number of access, this is not an element of the claimed invention. As such, the combination of Bogin and Woo still fails to teach or fairly suggest each and every element of the claimed invention. Because the combination of Bogin and Woo fails to teach each and every element of the claimed invention, Applicant therefore respectfully submits that the claimed invention (claims 1-12 and 20-27) is patentable over the combination of Bogin and Woo. Accordingly, Applicant respectfully requests that the Examiner reconsider and remove the rejection to claim 1-12 and 20-27.

CONCLUSION

Applicants submit that all grounds for objection and rejection have been properly traversed, accommodated, or rendered moot, and that the application is now in condition for allowance. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: June 6, 2006

Jan Little-Washington
Reg. No.: 41,181
(206) 292-8600

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